

## REMARKS

By this amendment, Applicants have amended independent claims 11, 13, 15 and 17 to recite that the insulating film(s) is (are) filled completely in the trench(es). See, e.g., Figure 23.

Applicants thank the Examiner, Long Pham, for the telephonic interview conducted between the Examiner and the undersigned on September 23, 2005. During the interview, the differences between the present invention and the Hirabayashi and Gocho et al. patents were discussed. The Examiner stated that he interprets the word "filled" in the claims to be the same as "buried" and to only require that the element isolation insulating films be at least partially contained in the trenches. Since the Examiner was not interpreting the word "filled" to mean completely filled, amending the claims to amend "filled" to --filled completely-- was discussed. The Examiner indicated this amendment appeared to distinguish over Hirabayashi. The Examiner indicated he would have to give further consideration as to whether the claims are allowable over the combination of Hirabayashi and Gocho et al., and would have to update his search.

Entry of this amendment under 37 CFR 1.116 is requested. Initially, it is submitted the foregoing amendments place the application in condition for allowance or, at least, in better form for consideration on appeal for the reasons set forth hereinafter. Moreover, the amendments are necessary and were not earlier presented since they are made in response to a new ground of rejection contained in the outstanding Office Action and in response to clarification of the Examining Attorney's position with respect to the word "filled" only recently made by the Examiner. Therefore, entry of this amendment under 37 CFR 1.116 is proper.

Claims 11-13, and 15-17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over by U.S. Patent No. 5,614,445 to Hirabayashi in view of U.S. Patent No. 5,498,565 to Gocho et al. Claim 14 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Hirabayashi. Applicants traverse these rejections and request reconsideration thereof.

Claims 11-17 are directed to a semiconductor integrated circuit device that has at least one trench formed in a semiconductor substrate and a defining active regions and dummy regions. An insulating film is filled completely in the at least one trench by polishing an insulating layer formed over the at least one trench and semiconductor substrate. According to the present invention, the dummy regions are formed at a scribing area so as to planarize a surface of the insulating film formed in the at least one trench at the scribing area by the polishing.

The patent to Hirabayashi discloses a process for manufacturing a semiconductor device which includes forming trench grooves in an integrated circuit region of a wafer and dummy etched grooves in a scribe line zone of a wafer. Both the trench grooves and the dummy etched grooves are provided with a sidewall insulating film on an inner sidewall and are filled with polycrystalline silicon to provide a smooth wafer surface. The wafer is then cleaved along the scribe line zone. The dummy etched grooves are provided so that the sum of the areas to be etched by dry etching accounts for not less than 5% of the total surface area on one side of the wafer.

In Hirabayashi, the insulating film 8 is formed only on the inner sidewalls of the trench and dummy grooves. The trench and dummy grooves of Hirabayashi are not filled completely with the insulating film 8. Rather, the trench grooves and dummy grooves of Hirabayashi are filled with polycrystalline silicon. Thus, the

Hirabayashi patent does not disclose an insulating film filled completely in a trench or insulating films filled completely in a plurality of trenches by polishing an insulating layer formed over the trench(es) and the semiconductor substrate, as presently claimed.

Moreover, the purpose of the dummy etched grooves of Hirabayashi is to make the sum of the areas to be etched not less than 5% of the whole area on one side of the semiconductor wafer so as to suppress side etching. On the other hand, the dummy regions of the present invention are formed at a scribing area so as to planarize a surface of the insulating films filled in the trenches at the scribing by the polishing. Since the purpose of the dummy etched grooves of Hirabayashi is completely different of that of the present invention, it is submitted there would have been no motivation to modify the teachings of Hirabayashi to arrive at the presently claimed invention.

The Gocho et al. patent discloses a method of forming trench isolation including a burying step of burying trenches by a deposition means for conducting etching and deposition simultaneously, and a polishing step of flattening a burying material by polishing conducted by disposing an isotropic etching step, a multi-layered etching stopper and a protrusion unifying structure. Polishing can be attained with satisfactory flatness uniformly or with no polishing residue even in a portion to be polished in which the etching stopper layer is distributed unevenly. The method can be applied to manufacture of a semiconductor device or the like.

Applicants submit there would have been no motivation to combine the teachings of Hirabayashi and Gocho et al. In Hirabayashi, an insulating material is not completely filled in the trenches. Therefore, it is not clear that the discussion at column 1, lines 30-55 of Gocho et al., noted by the Examiner, is at all relevant to the

disclosure of Hirabayashi. Accordingly, it is submitted there would have been no motivation to modify the Hirabayashi teachings to use the deposition and polishing steps of Gocho et al. Accordingly, the presently claimed invention is patentable over the proposed combination of Hirabayashi and Gocho et al.

In view of the foregoing amendments and remarks, entry of this amendment and favorable reconsideration and allowance of all of the claims now in the application are requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (Case: 1374.36127CC3), and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

  
\_\_\_\_\_  
Alan E. Schiavelli  
Registration No. 32,087

AES/at  
(703) 312-6600